portion of the first covering layer;

a third covering layer of semiconductor material of heavily doped first electrical conductivity type having a top surface and being contiguous to and partly overlying the top surface of the second covering layer, where a portion of the second covering layer is heavily doped and this portion extends vertically upward through the third covering layer to the top surface thereof and forms an exposed pattern of the second covering layer in the top surface of the third covering layer, and where the maximum depth of the heavily doped portion of the second covering layer relative to the top surface of the third covering layer is a depth d_1;

a trench having side walls and bottom walls and extending vertically downward from the top surface of the third covering layer through the third and second covering layers and through a portion of, but not all of, the first covering layer, where the trench has a maximum depth relative to the top surface of the third covering layer equal to a second depth d_2 and d_2 is less than d_1, where the trench in horizontal cross section is approximately a polygonal stripe, and where this polygonal stripe laterally surrounds and is spaced apart from the exposed pattern of the second covering layer at the top surface of the third covering layer;

a layer of oxide positioned within the trench and contiguous to the bottom walls and side walls of the trench so that portions, but not all, of the trench are filled with the oxide layer;

electrically conducting semiconductor material, contiguous to the oxide layer and positioned within the trench so that the oxide layer lies between the electrically conducting semiconductor material and the bottom and side walls of the trench; and

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

three electrodes that are electrically coupled to the electrically conducting semiconductor material in the trench, to the third covering layer and to the substrate, respectively;

wherein the difference d_1-d_2 of said first and second depths d_1 and d_2 is sufficient to force junction breakdown away from the trench and into the heavily doped portion of the second covering layer.

31. A trench DMOS transistor cell as in Claim 31, wherein said trench comprises rounded edges of oxidized material, where said bottom surfaces and said side surfaces of said trench meet said top surface of said third covering layer and where said side surfaces of said trench meet with one another.

32. A trench DMOS transistor cell, comprising:

a substrate;

an epitaxial layer above the substrate;

a trench in the epitaxial layer, the trench having a predetermined depth d_u; and

a body region in the epitaxial layer, the body region having a predetermined maximum depth d_{max},

wherein the depth d_u is less than the depth d_{max}, and

wherein the difference between the depth d_{max} and the depth d_u is sufficient to force junction breakdown away from the trench and into the epitaxial layer.

33. A trench DMOS transistor cell as in Claim 32, wherein the substrate is of a first conductivity type, the epitaxial layer is of said first conductivity type and the body region is of a second conductivity type.

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

~~34~~ 16. A trench DMOS transistor cell as in claim ~~33~~ wherein the epitaxial layer has a top surface and the body region extends from the epitaxial layer top surface into an upper portion of the epitaxial layer.

~~35~~ 18. A trench DMOS transistor cell as in claim ~~34~~ 17 wherein a source region is formed in said epitaxial layer.

~~36~~ 19. A trench DMOS transistor cell as in Claim ~~34~~ 17 wherein a ~~heavily doped~~ an epitaxial region partially covers the body region.

~~37~~ 20. A trench DMOS transistor cell as in Claim ~~36~~ 19 wherein the body region includes a heavily doped body region extending upward through the ~~heavily doped~~ epitaxial region and forming an exposed pattern at the epitaxial layer top surface.

~~38~~ 21. A trench DMOS transistor cell as in Claim ~~37~~ 20 wherein the trench surrounds the exposed pattern of the heavily doped body region.

~~39~~ 22. A trench DMOS transistor cell of Claim ~~32~~ 15 wherein the trench has side walls, said DMOS transistor cell having an oxide layer on said trench walls; and wherein said oxide layer is etched to create rounded corners in said trench.

~~40~~ 23. A trench DMOS transistor cell as in Claim ~~39~~ 22, further comprising a gate oxide layer within the trench.

~~41~~ 24. A trench DMOS transistor cell of Claim ~~40~~ 23 further comprising electrically conducting material contiguous to the gate oxide layer, wherein the gate oxide layer is located between the electrically conducting material and the trench.

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

42. A trench DMOS transistor as in Claim 40, further comprising:

a first polysilicon layer on a portion of said oxide layer;

a second oxide layer on a portion of said first polysilicon layer;

a second polysilicon layer on a portion of said second oxide layer; and

a metal layer wherein said second polysilicon layer extends from the trench to a field region creating an electrical contact to the metal layer and providing continuity from the metal layer to the trench.

43. A trench DMOS transistor cell as in Claim 32, further comprising an electrical contact to the gate region, the drain region and simultaneously to the body region and the source region.

44. A trench DMOS transistor cell as in Claim 32 wherein a horizontal cross section of the cell has a polygonal shape.

45. A trench DMOS transistor cell as in Claim 32 wherein a horizontal cross section of the cell has a substantially circular shape.

46. A transistor, comprising:

a first region of a first conductivity type;

a second region of a second conductivity type over said first region;

a third region of said first conductivity type such that said first and third regions are separated by said second region;

a trench through said third and second regions; and

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

a gate in said trench; wherein a portion P of said second region, which portion is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, an avalanche breakdown occurs away from a surface of said trench.

47. A transistor as in claim 46 wherein said portion P of said second region is doped heavier than another portion of said second region which portion is adjacent said trench.

48. A transistor as in Claim 46 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being lighter doped than said first portion.

49. A transistor as in Claim 48 wherein said avalanche breakdown is a reach-through breakdown across said second portion.

50. A transistor as in Claim 46 wherein said portion P of said second region extends deeper than said trench by more than 0.5 μm.

51. A transistor as in Claim 46 further comprising an insulator between said surface of said trench and said gate.

52. A transistor, comprising:

a region of a first conductivity type;

a second region of said first conductivity type over said first region, said second region being lighter doped than said first region;

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979